CLAIM LISTING:

1. (Currently Amended) A transistor comprising:

a device isolation film formed on a semiconductor substrate, the device isolation film having a groove that exposes a portion of the semiconductor substrate defining an active region and having a substantially vertical profile with respect to the exposed portion of the semiconductor substrate;

a gate electrode structure formed in a central portion of the active region of the semiconductor substrate and separated from the device isolation film, wherein the gate electrode structure further comprises:

a stacked structure of a gate oxide film, a first gate electrode and a second electrode, an oxide layer formed on a side wall of only the first gate electrode, and

nitride spacers formed on the oxide layer on the sidewall of the first gate electrode and on a side wall of the device isolation film;

lightly doped drain (LDD) regions formed in the active region of the semiconductor substrate on both sides of the gate electrode structure;

source/drain regions formed in the active region of the semiconductor substrate on both sides of the gate electrode structure; and

second and third insulating films filling and planarizing the space above the active region and between the first gate electrode structure and the device isolation film.

2. (Previously Presented) The transistor according to claim 1, wherein, the vertical profile of the device isolation film is modified near the junction of the device isolation film and the semiconductor substrate such that the device isolation film has a substantially rounded profile.

3. (Previously Presented) The transistor according to claim 1, further comprising a hard mask layer on the gate electrode structure.

4 – 6. (Cancelled)